JNTU-GV COLLEGE OF ENGINEERING VIZIANAGARAM (A)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY GURAJADA VIZIANAGARAM

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE STRUCTURE & SYLLABUS

M. Tech in VLSI Design and Embedded Systems Programme

(Applicable for batches admitted from 2025-2026)

I YEAR – I SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core – I	Digital System Design	3	1	0	4
Professional Core – II	CMOS Analog and Digital IC Design	3	1	0	4
Professional Core – III	Embedded Real Time Operating Systems	3	1	0	4
Professional Elective(s) – I	1. VLSI Architectures 2. Design for Testability 3. Physical Design and Verification 4. System Verilog	3	1	0	4
Professional Elective(s) – II	1. Embedded-C 2. Embedded Networking 3. Communication Busses and Interfaces 4. Image and Video Processing	3	1	0	4
Lab – I	Digital System Design Lab	0	1	2	2
Lab – II	Embedded Real Time Operating Systems Lab	0	1	2	2
	Seminar – I	0	0	2	1
	Total	**15**	**7**	**6**	**25**

I YEAR – II SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core – IV	Embedded System Design	3	1	0	4
Professional Core – V	CMOS Mixed Signal Circuit Design	3	1	0	4
Professional Core – VI	VLSI Signal Processing	3	1	0	4
Professional Elective(s) – III	1. Hardware Software Co-Design 2. Low Power VLSI Design 3. System on Chip (SoC) Design 4. Semiconductor Memory Design and Testing	3	1	0	4
Professional Elective(s) – IV	1. Internet of Things (IoT) 2. Artificial Intelligence & Machine Learning 3. Scripting Languages 4. Network Security and Cryptography	3	1	0	4
Lab – III	Embedded System Design Lab	0	1	2	2
Lab – IV	VLSI Design Lab	0	1	2	2
	Seminar – II	0	0	2	1
	Total	**15**	**7**	**6**	**25**

II YEAR – I SEMESTER

Course Code	Course Title	L	T	P	Credits
Open Elective	Research Methodology and IPR / SWAYAM MOOCS course – RM & IPR	2	0	0	2
	Summer Internship / Industrial Training	0	0	0	2
Dissertation	Dissertation Part – A	0	0	20	10
	Total	**2**	**-**	**20**	**14**

II YEAR – II SEMESTER

Course Code	Course Title	L	T	P	Credits
Dissertation	Dissertation Part – B	0	0	32	16
	Total	**0**	**0**	**32**	**16**

	L	T	P	C
M. Tech I- Year I- Semester	3	1	0	4

Digital System Design

Course Objectives:

- To provide extended knowledge of digital logic circuits in the form of state model approach.
- To provide an overview of system design approach using programmable logic devices.
- To provide and understand of fault models and test methods.
- To get exposed to the various architectural features of CPLDS.
- To learn the methods and techniques of CPLD design with EDA tools

UNIT-I:

Minimization Procedures and CAMP Algorithm: Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II:

PLA Design, Minimization and Folding Algorithms: Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm (COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -III:

Design of Large-Scale Digital Systems: Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV:

Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V:

Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

Textbooks:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi, 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

Reference Books:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Monobaraminic, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

Course Outcomes:

- To provide in depth understanding of Fault models.
- To understands test pattern generation techniques for fault detection.
- To design fault diagnosis in sequential circuits.
- To provide understanding in the design of flow using case studies.

	L	T	P	C
M. Tech I- Year I- Semester	3	1	0	4

CMOS Analog and Digital IC Design
(Elective-II)

Course Objectives:

- ❖ Understand how MOS transistors work and how they are used in circuits.
- ❖ Learn how to design digital logic circuits (like AND, OR, and flip-flops) using MOS technology.
- ❖ Study advanced MOS circuit types, such as dynamic logic and memory circuits like RAM and flash.
- ❖ Explore analog MOS circuits, including how to build current sources and voltage references.
- ❖ Learn how CMOS amplifiers and operational amplifiers are designed and used.

UNIT-I:

MOS Devices and Modelling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modelling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II:

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT -III:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

UNIT -IV:

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT-V:

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

Textbooks:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH,3rd Ed., 2011.
3. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
4. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R.G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2016.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
4. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

Course Outcomes:

- ❖ Explain and model MOS devices using large-signal, small-signal, and computer simulation models.
- ❖ Design digital logic circuits (combinational and sequential) using NMOS, CMOS, and transmission gates.
- ❖ Analyze and design memory circuits like SRAM, DRAM, and flash memory, understanding their structure and behavior.
- ❖ Build analog sub-circuits such as current mirrors and voltage references using CMOS.
- ❖ Design and evaluate CMOS amplifiers and operational amplifiers, including multi-stage and high-gain architectures.

M. Tech I- Year I- Semester	L	T	P	C
	3	1	0	4

Embedded Real Time Operating Systems

Course Objectives:

- Introduce basic UNIX/Linux commands and system calls used for file handling and process control.
- Explain what Real-Time Operating Systems (RTOS) are, their features, and how they handle tasks.
- Teach about communication and synchronization tools like semaphores and message queues used in RTOS.
- Explore system-level components such as signals, timers, and interrupts in real-time systems.
- Provide real-world examples of RTOS through case studies of popular systems like RT Linux and VxWorks.

UNIT – I: Introduction

Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II: Real Time Operating Systems

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III: Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/ O Subsystem

UNIT - IV: Exceptions, Interrupts and Timers

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Textbooks:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

Reference Books:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

Course Outcomes:

- ❖ Use basic UNIX/Linux commands and system calls to manage files and processes.
- ❖ Understand how RTOS schedules tasks and manages concurrency using semaphores and queues.
- ❖ Explain the working of core RTOS components, including events, signals, pipes, and I/O subsystems.
- ❖ Analyze how interrupts and timers work in a real-time environment.
- ❖ Compare different RTOS platforms like RT Linux, MicroC/OS-II, and Android, understanding their structure and use.

M. Tech I- Year I- Semester	**L**	**T**	**P**	**C**
	3	1	0	4

VLSI Architectures

(Professional Elective-I)

Course Objectives:

- To understand programmable logic devices (CPLD/FPGA) and their internal architectures.
- To analyze and compare CPLD/FPGA device families and performance.
- To study finite state machine (FSM) design methodologies and implementation strategies.
- To apply FSM architectures such as one-hot and ASM methods for digital design and develop system-level designs with controller, datapath, and functional partitioning.

UNIT–I:

Programmable Logic Devices: Complex Programmable Logic Devices (CPLD): ROM, PLA, PAL, PLD, PGA – Features, programming and applications, Altera MAX 5000/7000 series, Altera FLEX 10000 series CPLD, AMD's CPLD (Mach 1–5), Cypress FLASH 370 device technology, Lattice LSI's 3000 series – Speed, performance, in-system programmability. Introduction to FPGAs: Logic blocks, routing architecture, design flow, technology mapping.

UNIT–II:

FPGA/CPLD Architectures: FPGA/CPLD device architectures: Xilinx XC4000 series, Altera FLEX 8000/10000 series, AT&T ORCA (Optimized Reconfigurable Cell Array), Actel ACT-1, ACT-2, ACT-3 families Comparison of architectures with respect to speed, performance, and area trade-offs.

UNIT–III:

Finite State Machines (FSM) Top-down FSM design, state transition tables, state assignment for FPGAs, Initial state assignment for one-hot encoding, Realization of state machine charts with PAL, Alternative realization using microprogramming, Linked state machines One-hot state machines, Petri nets for FSM design – concepts, properties, and parallel controllers, Meta-stability and synchronization issues, **Case Study:** FSM-based digital system design.

UNIT–IV:

Architectures centered around non-registered PLDs, FSM design using shift registers,One-hot design method and its applications, use of Algorithmic State Machines (ASM) in one- hot design Advantages and trade-offs of FSM-based architecture.

UNIT–V:

System-level partitioning: Controller, datapath, and functional partitions, design of parallel adder cells and sequential circuits, counters, multiplexers, and system controllers, parallel controllers for high-performance designs, application-oriented system design using FPGAs/CPLDs.

Textbooks:

1. Digital Design with CPLD Applications and VHDL Delmar Cengage Learning, 2004.
2. Digital Systems Design Using VHDL – Charles H. Roth Jr., Lizy Kurian John Cengage Learning, 2017.
3. Field-Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems – Stephen M. Trimberger Springer, 1994.

Reference Books:

1. Digital Design and Computer Architecture – David Harris, Sarah Harris Morgan Kaufmann, 2012.
2. VHDL: Programming by Example – Douglas L. Perry McGraw Hill, 2002

e-Resources:

1.https://www.youtube.com/playlist?list=PLfMCiCIRnpUnFgNSy0QuOuqIIrG0fe5eD

Course Outcomes:

- Explain programmable logic device architectures (CPLD, FPGA) and their applications.
- Analyze FPGA/CPLD architectures and evaluate their speed and performance.
- Design finite state machines using PLDs and apply advanced techniques such as one-hot encoding and ASM charts.
- Develop system-level digital designs using controller–datapath partitioning and functional modules.

	L	T	P	C
M. Tech I- Year I- Semester	3	1	0	4

Design for Testability

(Professional Elective-I)

Course Objectives:

- Introduce fault models and basic faults in digital systems.
- Explain stuck-at fault testing and design for testability techniques.
- Develop skills to analyze testing issues in digital circuit design.
- Enable modeling and simulation of faults for reliable circuit performance.
- Encourage research on advanced testing methods for digital and mixed-signal systems.

UNIT -I

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:

Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III:

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test- Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.

Reference Books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Course Outcomes:

- Demonstrate advanced knowledge in the basic faults that occur in digital systems, testing of stuck at faults for digital circuits, Design for testability.
- Analyse testing issues in the field of digital system design critically for conducting research.
- Solve engineering problems by modelling different faults for fault free simulation in digital circuits.
- Apply appropriate research methodologies and techniques to develop new testing strategies for digital and mixed signal circuits and systems.

M. Tech I- Year I- Semester	L	T	P	C
	3	1	0	4

Physical Design and Verification

(Professional Elective-I)

Course Objectives:

- To understand the VLSI design and physical design cycles, including fabrication and layout processes.
- To explore design styles and interconnect issues, focusing on noise, crosstalk, and yield.
- To study graph algorithms and data structures for solving physical design problems.
- To learn partitioning, floor planning, and routing algorithms for efficient VLSI design.

UNIT- I

VLSI Design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication. Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi- Chip Modules. Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.

UNIT- II

Factors, Complexity Issues and NP-hard Problems. Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.

UNIT- III

Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbour Pointers, Corner Stitching, Multi-Layer Operations.

UNIT- IV

Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.

UNIT- V

Partitioning Algorithms: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Routing and Placement Algorithms.

Textbooks:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

Reference Books:

1. "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Harris.
2. "VLSI Physical Design: From Graph Partitioning to Timing Closure" by K. D. Meade and L. F. D. DeMicheli.

e-Reference:

NPTEL Courses (**https://nptel.ac.in/courses/106103016**)

Course Outcomes:

- ❖ Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology.
- ❖ Adapt the design algorithms to meet the critical design parameters.
- ❖ Identify layout optimization techniques and map them to algorithms.
- ❖ Develop proto-type EDA tool and test its efficacy

M. Tech I- Year I- Semester	L	T	P	C
	3	1	0	4

System Verilog

(Professional Elective-I)

Course Objectives:

- Learn the basic ideas of verification methods and System Verilog data types.
- Understand how to use procedural statements, routines, and assertions in verification.
- Learn the basic concepts of object-oriented programming (OOP) in SystemVerilog.
- Practice using randomization techniques to test designs.
- Learn how to use functional coverage to check how well the design is verified.

UNIT I: Verification guidelines and Data types.

Verification guidelines: Verification Process, Basic Test bench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Test bench components, layered test bench, Building layered test bench.

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative Arrays, linked lists, Array methods, choosing a storage type, creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants, strings, expression width.

UNIT-II: Routines and Connecting the test bench & design.

Procedural statements and routines: Procedural statements, tasks, functions and void Functions, Routine arguments, returning from routine, local data storage, Time values. Connecting the test bench and design: Separating the test bench and design, Interface constructs, Stimulus timing, Interface driving and sampling, connecting it all together, Top-level scope, Program – Module interactions, System Verilog assertions.

UNIT-III: Basic OOP

Introduction, first class, define a class, OOP (Object Oriented Programming) terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, scoping rules, using one class inside another, understanding dynamic objects, Copying objects, Public vs. private, straying off course, building a test bench.

UNIT- IV: Randomization

Introduction, randomization, Randomization in System Verilog, Constraint details, solution probabilities, controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre-randomize and post randomize functions, Constraints tips and techniques, common randomization problems.

UNIT-V: Interprocess communication and Functional Coverage

Interprocess Communication, Events, Semaphores, Mailboxes, Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation.

Textbook:

1. Chris Spear, System Verilog for Verification, 2ndEdition, Springer, 2008.
2. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan, “A practical guide for System Verilog assertions”, Springer Science & Business Media, 2006.

Reference Books:

1. Bergeron, Janick, “Writing testbenches using System Verilog”, 1stEdition, Springer Science &Business Media, 2007.

Course Outcomes:

- ❖ Understand verification methods and data types.
- ❖ Explain procedural statements, routines, and assertions.
- ❖ Describe basic OOP terms in System Verilog.
- ❖ Use randomization for design verification.
- ❖ Understand and apply functional coverage concepts.

M. Tech I- Year I- Semester	L	T	P	C
	3	1	0	4

Embedded-C

(Professional Elective-II)

Course Objectives:

- Introduce the fundamental programming concepts relevant to embedded system design.
- Explain the features, syntax, and semantics of embedded programming languages.
- Describe the structure, architecture, and operation of microcontroller-based embedded systems.
- Develop the ability to design, code, and debug simple programs for embedded hardware.

UNIT – I:

Programming Embedded Systems in C: Introduction, what is an embedded system, Which processor should you use, which programming language should you use, Which operating system should you use, how do you develop embedded software, Conclusions. Introducing the 8051 Microcontroller Family Introduction, what's in a name, the external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions.

UNIT – II:

Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

UNIT – III:

Adding Structure to the Code: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

UNIT – IV:

Meeting Real-Time Constraints: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions.

UNIT – V:

Case Study: Intruder Alarm System Introduction, the software architecture, Key software components used in this example, running the program, the software, Conclusions.

Textbook:

1. Embedded C by Michael J. Pont, A Pearson Education.

Reference Books:

2. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C By Nigel Gardner.

Course Outcomes:

- Know about programming concepts in embedded system design
- Understand features and concepts of embedded programming languages
- Able to describe how microcontroller based embedded systems are programmed and implemented in real time applications.
- Write simple programs and implement the same embedded hardware

M. Tech I- Year I- Semester	L	T	P	C
	3	1	0	4

Embedded Networking

(Professional Elective-II)

Course Objectives:

- To introduce the Building Blocks of Embedded System.
- To Educate in Various Embedded Development Strategies.
- To Introduce Bus Communication in processors, Input/output interfacing.
- To impart knowledge in various processor scheduling algorithms.
- To introduce Basics of Real time operating system and example tutorials to discuss on one real time operating system tool.

UNIT –I: Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II:

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III:

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol. UNIT –IV: Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V:

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Textbooks:

1. Embedded systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference Books:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari? Cambridge press 2005.

Course Outcomes:

- ❖ Acquire a basic knowledge about fundamentals of microcontrollers
- ❖ Acquire a basic knowledge about programming and system control to perform a specific task.
- ❖ Acquire knowledge about devices and buses used in embedded networking
- ❖ Develop programming skills in embedded systems for various applications.
- ❖ Acquire knowledge about basic concepts of circuit emulators.

M. Tech I- Year I- Semester	L	T	P	C
	3	1	0	4

Communication Busses and Interfaces

(Professional Elective-II)

Course Objectives:

- Understand the basics of serial buses and compare them with parallel communication.
- Study protocols like RS232, RS485, I2C, and SPI with focus on features and limitations.
- Explore CAN bus architecture, layers, frame formats, and real-time applications.
- Learn PCIe and USB protocols, including configuration, transfer types, and descriptors.
- Understand serial data streaming using SFPDP and its transmission techniques.

UNIT I

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features Limitations and applications of RS232, RS485, I2C, SPI.

UNIT II

CAN: Architecture- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame Formats-Data frame, Remote frame, Error frame, Overload frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT III

PCIe: Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IV

USB: Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT V

Data streaming Serial Communication Protocol- Serial Front Panel Data Port (SFPDP) configurations, Flow control, serial FPDP transmission frames, fibre frames and copper cable.

Textbooks:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded Systems-Jan Axelson, Lakeview Research, 2nd Ed.

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

Course Outcomes:

- ❖ Identify and compare different serial and parallel communication protocols.
- ❖ Explain working and applications of RS232, RS485, I2C, and SPI.
- ❖ Describe CAN architecture, layers, and frame formats used in communication.
- ❖ Demonstrate knowledge of PCIe and USB protocol operations and configurations.
- ❖ Apply serial data streaming methods using SFPDP for high-speed communication

	L	T	P	C
M. Tech I- Year I- Semester	3	1	0	4

Image and Video Processing

(Professional Elective-II)

Course objectives:

- To study the image fundamentals and mathematical transforms necessary for image processing.
- To study the image enhancement techniques
- To study image restoration procedures.
- To study the image compression procedures.

UNIT –I:

Fundamentals of Image Processing and Image Transforms: Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing.

Introduction, need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT –II:

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Restoration: Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT –III:

Image Segmentation: Introduction to image segmentation, Point, Line and Edge Detection, Region based segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

Image Compression: Introduction, need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding, Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression, JPEG Standards.

UNIT -IV:

Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V:

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

Textbooks:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.
3. S. Jayaraman, S. Esakkirajan and T. Veera Kumar, "Digital Image processing, Tata McGraw Hill publishers, 2009.

Reference Books:

1. Digital Image Processing and Analysis-Human and Computer Vision Application with CVIP Tools – Scotte Umbaugh, 2nd Ed, CRC Press, 2011.
2. Digital Video Processing – M. Tekalp, Prentice Hall International.
3. Multi-dimensional Signal, Image and Video Processing and Coding – John Woods, 2nd Ed, Elsevier.
4. Digital Image Processing with MATLAB and Labview – Vipula Singh, Elsevier.

Course Outcomes

- Review the fundamental concepts of a digital image processing system.
- Analyze images in the frequency domain using various transforms.
- Evaluate the techniques for image enhancement and image restoration.
- Categorize various compression techniques and Interpret Image compression standards
- Interpret image segmentation and representation techniques.

M. Tech I- Year I- Semester	L	T	P	C
	0	1	2	2

Digital System Design Lab

Course Objectives:

- Introduce key algorithms for logic minimization and circuit optimization.
- Familiarize students with ROM and PLA design techniques.
- Develop understanding of control unit and data path design.
- Provide hands-on experience with FPGA-based digital system design.
- Explore fault detection and correction using algorithms like Kohavi and Hamming.

Systems Design experiments:

- The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
- Consider the suitable switching function and data to implement the required logic if required.

A student has to do at least 10 Experiments.

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm)
5. PLA folding algorithm (COMPACT algorithm)
6. ROM design.
7. Control unit and data processor logic design
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.

Course Outcomes:

- Apply CAMP-I and CAMP-II algorithms to determine EPCs, SPCs, and SCs.
- Implement PLA minimization and folding using IISc and COMPACT algorithms.
- Design ROMs and analyze their role in digital systems.
- Design and simulate control units and data processors.
- Use FPGA tools and implement error detection using Kohavi and Hamming codes.

	L	T	P	C
M. Tech I- Year I- Semester	0	1	2	2

Embedded Real Time Operating Systems Lab

Course Objectives:

- To develop applications using task scheduling, timers, and event-driven programming in embedded systems.
- To implement and analyze inter-task communication mechanisms such as message queues, mailboxes, and interrupts.
- To demonstrate task synchronization, time slicing, and priority-based scheduling.
- To interface and control peripherals like LEDs, LCDs, serial ports, and audio processing units.
- To enhance practical understanding of real-time operating systems (RTOS) concepts through hands-on experiments.

Note: The following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task.
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have
4. higher priority than external interrupt button)
   a). Write an application to Test message queues and memory blocks.
   b). Write an application to Test byte queues.
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different Timings
7. Write an application that creates a two-task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

Course Outcomes:

- Apply inter-task communication techniques such as message queues, mailboxes, and interrupts for efficient data exchange.
- Demonstrate task synchronization and scheduling through time slicing and priority-based execution.
- Develop and interface embedded applications using peripherals like LEDs, LCDs, serial communication, and audio processing.
- Analyze and evaluate real-time operating system (RTOS) concepts through practical hands-on experiments.

M. Tech I-Year II- Semester	L	T	P	C
	3	1	0	4

Embedded System Design

Course Objectives:

- To understand the lifecycle of embedded systems
- To analyze and design hardware and software components
- To explore real-time operating systems, drivers, and middleware
- To implement and test real embedded applications
- To gain hands-on exposure to industry-relevant platforms

UNIT-I

The Embedded System Design Life Cycle:

Introduction, product specification, embedded systems architecture, embedded system design flow, embedded systems model, hardware/software partitioning, iteration and implementation, detailed hardware and software design, hardware/software integration, product testing and release. the golden rules of architectural embedded systems design: engineering approach.

UNIT-II

Embedded Hardware Design:

Embedded hardware building blocks, Embedded processors: ISA architecture models, internal processor design, processor performance, Board Memory: ROM, RAM, auxiliary memory, memory management of external memory, board memory and performance, Embedded board Input / output: serial versus parallel I/O, interfacing the I/O components, I/O components and performance, Board buses: Bus arbitration and timing, Integrating the bus with other board components, bus performance.

UNIT-III

Embedded Software Design:

Device drivers: Device drivers for interrupt handling, memory device drivers, on-board bus device drivers, Board I/O driver examples, Embedded operating systems: Multitasking and process management, memory management, I/O and file system management, OS standards example, OS performance guidelines, selecting the right embedded OS and BSPs, Middleware and application software: Middle ware, middleware examples, application layer software examples.

UNIT-IV

Embedded System Design Development, Implementation and Testing:

The development environment: The execution environment, memory organization, system start-up, creating an embedded system architecture, special software techniques: manipulating the hardware, interrupts and ISRs, watchdog timers, flash memory, design methodology,

getting embedded software into the target system, the ICE, Implementing the design: The main software utility tool, CAD and the hardware, Testing: choosing test cases, testing embedded hardware, performance and testing, maintenance and testing.

UNIT-V

Embedded System Design - Case Studies:

Case studies- Processor design approach of an embedded system –Power PC processor based and Micro Blaze processor based embedded system design on Xilinx platform, NiosII Processor based Embedded system design on Altera Platform- respective processor architectural issues are required to be consider while an embedded system design.

Textbooks:

1. Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers - Tammy Noergaard, Second Edition, Elsevier (Singapore) Private Limited Publications, 2005.
2. Embedded Systems Design: An Introduction to Processes, Tools & Techniques - Arnold S.Berger, Elsevier CMP Books, 2010.

Reference Books:

1. Embedded system Design: A Unified Hardware/Software Introduction - J Frank Vahid, Tony D. Givargis, John Wily & Sons Inc.2002.
2. Embedded Systems: Architecture, Programming and Design - Rajkamal, TMH, Second Edition, 2008.

Course Outcomes:

- ❖ Develop embedded systems from specification to deployment
- ❖ Use modern tools (hardware/software) for embedded design
- ❖ Design efficient systems with proper hardware/software balance
- ❖ Test, debug, and optimize embedded systems
- ❖ Apply knowledge in platform-based designs using Xilinx or Altera

	L	T	P	C
M. Tech I-Year II- Semester	3	1	0	4

CMOS Mixed Signal Circuit Design

Course Objectives

- ❖ Understand the fundamentals of phase-locked loops (PLLs) and key circuit components such as comparators and analog multipliers.
- ❖ Learn the principles of sampling circuits, including sample-and-hold architectures and switching methods.
- ❖ Explore the operation and architectures of digital-to-analog converters (DACs) and their performance characteristics.
- ❖ Study analog-to-digital converters (ADCs), quantization effects, and major converter types.
- ❖ Examine filter design using integrators and analyze various active and MOSFET-based filter topologies.

UNIT- I:

Phase Locked Loop: Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL.

UNIT -II:

Sampling Circuits Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures- Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

UNIT- III:

D/A Converter Architectures Input/output characteristics of an ideal D/A converter, , performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, , switching functions to generate an analog output corresponding to a digital input. Resistor-Ladder architectures, Current steering architectures.

UNIT -IV:

A/D Converter Architectures Input/output characteristics and quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures, interleaved architectures.

Unit -V:

Integrator Based Filters Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-c integrator, and discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

Textbooks:

1. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, Edition 2002.
2. Razavi, “Principles of data conversion system design”, Wiley IEEE Press, 1st Edition, 1994.
3. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2009.

Reference Books:

1. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”, John Wiley & Sons, 1986.
2. Baker, Li, Boyce, “CMOS: Circuit Design, layout and Simulation”, PHI, 2000.

Course Outcomes

- ❖ Design and explain PLL circuits and describe their key applications in electronics.
- ❖ Analyze and compare different sampling and sample-hold circuits used in analog signal processing.
- ❖ Select and explain suitable DAC architectures for converting digital signals into analog signals in electronic systems.
- ❖ Identify and apply different ADC architectures to convert analog inputs into digital signals accurately.
- ❖ Design and implement basic analog filters using integrator circuits and understand how different filter topologies work.

M. Tech I-Year II- Semester	L	T	P	C
	3	1	0	4

VLSI Signal Processing

Course Objective:

- Introduce fundamental concepts and algorithms of Digital Signal Processing (DSP), emphasizing pipelining and parallel processing benefits.
- Apply folding and unfolding techniques to optimize digital systems for reduced registers and delays.
- Explain systolic architectures for efficient array-based processing in filtering and matrix operations.
- Explore fast convolution methods, including Cook-Toom and Winograd algorithms, for high-speed signal processing.
- Discuss digital filter structures, bit-level optimization, and power-efficient DSP design strategies.

UNIT -I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multi rate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipelines, low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Textbooks:

1. Keshab K. Parthi[A1], VLSI Digital signal processing systems, design and implementation[A2], Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994 3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

Course Outcomes:

- Ability to modify the existing or new DSP architectures suitable for VLSI.
- Understand the concepts of folding and unfolding algorithms and applications.
- Ability to implement fast convolution algorithms.
- Low power design aspects of processors for signal processing and wireless applications.

	L	T	P	C
M. Tech I-Year II- Semester	3	1	0	4

Hardware Software Co-Design

(Professional Elective-III)

Course Objectives:

- Understand co-design models, architectures, and partitioning methods.
- Learn prototyping, emulation techniques, and system communication architectures.
- Explore modern embedded architectures and compilation tools.
- Study specification and verification methods in system design.
- Gain knowledge of system-level design languages and co-simulation tools.

UNIT-I:

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II:

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I: System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and Lycos system.

Textbooks:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Course Outcomes:

- Explain co-design models, synthesis algorithms, and HW/SW partitioning.
- Describe prototyping and emulation methods for system design.
- Identify tools and techniques used for compiling embedded software.
- Apply design and verification concepts in embedded system development.
- Use system-level specification languages and simulate multi-language designs.

M. Tech I-Year II- Semester	L	T	P	C
	3	1	0	4

Low Power VLSI Design

(Professional Elective-III)

Course Objectives:

- To understand the different leakage power reduction techniques.
- To impart knowledge on different abstraction levels in VLSI Design and the impact of power minimization methods at higher levels
- To explain technology independent and technology-dependent techniques for power reduction in CMOS circuits
- To introduce various software power estimation and optimization techniques for low power VLSI system design

UNIT –I:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.

Course Outcomes:

- Demonstrate knowledge on different sources of power dissipation, power minimization techniques, switched capacitance minimization and working principle of adiabatic logic circuits
- Designing low voltage CMOS circuits to reduce power consumption and low energy circuits.
- Analyze and minimize dynamic and static power consumption in VLSI circuits.
- Discover different ways to minimize leakage power and to achieve low power using voltage scaling, software design.

M. Tech I-Year II- Semester	L	T	P	C
	3	1	0	4

System On Chip (SoC) Design
(Professional Elective-III)

Course Objectives:

- To understand the concepts of SOC Testing.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.

UNIT I

System Architecture: Overview: Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design iteration – System Architecture & complexity – Product Economics for SOC-Dealing with Design Complexity

UNIT II

Processor Selection for SOC: Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT III

Memory Design: SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and Dcaches – multilevel caches – SoC memory systems – board-based memory systems – simple processor/memory interaction.

UNIT IV

Interconnect Architectures and SOC Customization: Bus architectures – SoC standard buses – AMBA, Core Connect – Bus Interface Units: Bus Sockets and Bus Wrappers– Contention and Shared Bus-SOC Customization: An Overview-Processor Customization Approaches -Reconfigurable Technologies

UNIT V

Application Studies: SOC Design Approach, AES: Algorithm and Requirements, AES: Design and Evaluation, 3-D Graphics Processors-Analysis: Processing-Analysis: Interconnection-Prototyping, JPEG Compression, Example JPEG System for Digital Still Camera.

Textbooks

1. Flynn, Michael J., and Wayne Luk. *Computer system design: system-on-chip*. John Wiley & Sons, 2011.
2. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
3. Wayne Wolf, "Modern VLSI Design – IP based Design", Prentice Hall, 4th Edition, 2008.

Course Outcomes:

- ❖ Upon successful completion of the program the students shall
- ❖ Explain all important components of a System-on-Chip
- ❖ Understanding the Processor selection for SOC Design
- ❖ Outline the major Memory Design Challenges.
- ❖ Discuss about SOC Customization Explore Different SOC Applications

		L	T	P	C
M. Tech I-Year II- Semester		3	1	0	4

Semiconductor Memory Design and Testing

(Professional Elective-III)

Course Objective:

- Understand Semiconductor Memory Fundamentals
- Explore Non-Volatile Memory Technologies
- Develop Skills in Memory Testing and Fault Tolerance
- Evaluate Memory Reliability and Radiation Effects
- Investigate Advanced and Future Memory Technologies

UNIT-I

Random Access Memory Technologies: SRAM –SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT -II:

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One-time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT -III:

Memory Fault Modelling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modelling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modelling and testing, IDDQ fault modelling and testing, Application specific memory testing, RAM fault modelling, BIST techniques for memory.

UNIT -IV:

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modelling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT -V:

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Textbooks:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications – Ashok K. Sharma2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall

Course Outcomes:

- Analysis the different types of RAM, ROM designs.
- Analysis the different RAM and ROM architecture and interconnects.
- Analysis about design and characterization technique.
- Analysis of different memory testing and design for testability.
- Identification of new developments in semiconductor memory design

	L	T	P	C
M. Tech I-Year II- Semester	3	1	0	4

Internet of Things (IoT)

(Professional Elective-IV)

Course Objectives:

- ❖ To Understand Smart Objects and IoT Architectures.
- ❖ To learn about various IOT-related protocols
- ❖ To build simple IoT Systems using Arduino and Raspberry Pi.
- ❖ To understand data analytics and cloud in the context of IoT
- ❖ To develop IoT infrastructure for popular applications.

UNIT I:

Fundamentals Of IOT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures, oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.

UNIT II:

IOT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT III:

Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT IV:

Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT V:

Case Studies/Industrial Applications: Cisco IoT system, IBM Watson IoT platform, Manufacturing, Converged Plant wide Ethernet Model (CPwE), Power Utility Industry, Grid Blocks Reference Model, Smart and Connected Cities: Layered architecture, Smart Lighting, Smart Parking Architecture and Smart Traffic Control.

Textbooks:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.

Reference Books:

1. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015
2. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Ho¨ ller, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
4. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.
5. Recipes to Begin, Expand, and Enhance Your Projects, 2nd Edition, Michael Margolis, Arduino Cookbook and O'Reilly Media, 2011.

Course Outcomes:

- Summarize on the term 'internet of things' in different contexts.
- Analyze various protocols for IoT.
- Design a PoC of an IoT system using Rasperry Pi/Arduino
- Apply data analytics and use cloud offerings related to IoT.
- Analyze applications of IoT in real time scenario

	L	T	P	C
M. Tech I-Year II- Semester	3	1	0	4

Artificial Intelligence & Machine Learning

(Professional Elective-IV)

Course Objectives:

- Gain a historical perspective of Artificial Intelligence (AI) and its foundations.
- Become familiar with basic principles of AI toward problem solving, inference, perception, knowledge representation, and learning.
- Develop an appreciation for what is involved in learning from data.
- Demonstrate a wide variety of learning algorithms.
- Demonstrate how to apply a variety of learning algorithms to data.

UNIT-I:

Introduction to artificial intelligence: Introduction, history, intelligent systems, foundations of AI, applications, tic-tac-tie game playing, development of AI languages, current trends in AI, Problem solving state-space search and control strategies: Introduction, general problem solving, characteristics of problem, exhaustive searches, heuristic search techniques, iterative deepening a*, constraint satisfaction

UNIT-II:

Problem reduction and game playing: Introduction, problem reduction, game playing, alpha beta pruning, two-player perfect information games, Logic concepts: Introduction, propositional calculus, proportional logic, natural deduction system, axiomatic system, semantic tableau system in proportional logic, resolution refutation in proportional logic, predicate logic

Knowledge representation: Introduction, approaches to knowledge representation, knowledge representation using semantic network, extended semantic networks for KR, knowledge representation using frames, advanced knowledge representation techniques: Introduction, conceptual dependency theory, script structure, cyc theory, case grammars, semantic web.

UNIT-III:

Fuzzy sets and fuzzy logic: Introduction, fuzzy sets, fuzzy set operations, types of membership functions, multi valued logic, fuzzy logic, linguistic variables and hedges, fuzzy propositions, inference rules for fuzzy propositions, fuzzy systems.

Introduction to Machine Learning: Introduction-Towards Intelligent Machines, Well posed Problems, Example of Applications in diverse fields, Data Representation, Domain Knowledge for Productive use of Machine Learning, Diversity of Data: Structured

/ Unstructured, Forms of Learning, Machine Learning and Data Mining, Basic Linear Algebra in Machine Learning Techniques.

UNIT-IV:

Supervised Learning- Rationale and Basics: Learning from Observations, Bias and Why Learning Works: Computational Learning Theory, Occam's Razor Principle and Overfitting Avoidance Heuristic Search in inductive Learning, Estimating Generalization Errors, Metrics for assessing regression, Metris for assessing classification.

UNIT-V:

Statistical Learning- Machine Learning and Inferential Statistical Analysis, Descriptive Statistics in learning techniques, Bayesian Reasoning: A probabilistic approach to inference, K-Nearest Neighbor Classifier. Discriminant functions and regression functions, Linear Regression with Least Square Error Criterion, Logistic Regression for Classification Tasks, Fisher's Linear Discriminant and Thresholding for Classification, Minimum Description Length Principle.

Textbooks:

1. Artificial Intelligence, A modern Approach, 2nd ed, Stuart Russel, Peter Norvig, Prentice Hall
2. Artificial Intelligence, Saroj Kaushik, 1st Edition, CENGAGE Learning, 2011.
3. Applied Machine Learning, M. Gopal, McGraw Hill Education, 2019.
4. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press,2012.

Reference Books:

1. Artificial intelligence, structures and Strategies for Complex problem solving, 5th Edition, George F Lugar, PEA
2. Introduction to Artificial Intelligence, Ertel, Wolf Gang, Springer, 2017
3. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, Springer 2009 (freely available online)
4. Christopher Bishop, Pattern Recognition and Machine Learning, Springer,2007.

Course Outcomes:

- Demonstrate knowledge of the building blocks of AI as presented in terms of intelligent agents.
- Analyze and formalize the problem as a state space, graph, design heuristics and select amongst different search or game-based techniques to solve them.
- Domain Knowledge for Productive use of Machine Learning and Diversity of Data.
- Demonstrate on Supervised and Computational Learning
- Analyze on Statistics in learning techniques and Logistic Regression

M. Tech I-Year II- Semester	L	T	P	C
	3	1	0	4

Scripting Languages

(Professional Elective-IV)

Course Objectives:

- To introduce the fundamentals of scripting languages and their role in VLSI design automation.
- To describe PERL concepts for handling large data sets in VLSI/CAD applications.
- To utilize TCL for CAD tool interfacing and automation.
- To interpret the PYTHON language and its role in design, testing, and application development.

UNIT- I: Introduction to Scripts and Scripting

Basics of Linux, Origin of scripting languages, Characteristics, Uses of scripting languages, Applications in VLSI and CAD tools.

Unit-II: PERL Basics

Introduction to PERL, Names and values, Variables and assignments, Scalar expressions, Control structures, Built-in functions, Arrays, Lists, and Hashes, Simple Input/Output, Strings, Regular Expressions, Subroutines, Command-line arguments.

Unit-III: Advanced PERL

Looping structures, Advanced Subroutines, Pack and Unpack, File handling, Type globs, Eval and References, Data structures, Packages, Libraries, and Modules, Object-Oriented PERL, Tied Variables, OS Interfacing, Security Issues.

Unit-IV: TCL Programming

TCL phenomena, Philosophy and structure, Syntax and Parser, Variables and data types, Control flow, Data structures, Input/Output, Procedures, String handling, Patterns, File and Pipe handling, Example applications in EDA.

Unit-V: PYTHON Programming

Introduction to PYTHON, Syntax and Statements, Functions, Built-in Functions and Methods, Modules, Exception Handling, Applications of PYTHON in VLSI, system development, and web applications.

Textbooks:

1. David Barron, *The World of Scripting Languages*, Wiley Student Edition, 2010.
2. Steve Holden, David Beazley, *PYTHON Web Programming*, New Riders Publications, 2012.

Reference Books:

1. Clif Flynt, *TCL/TK: A Developer's Guide*, Morgan Kaufmann, 2003.
2. Chun, *Core PYTHON Programming*, Pearson Education, 2006.
3. Randal L. Schwartz, *Learning PERL*, O'Reilly Publications, 6th Edition, 2011.
4. Richard Peterson, *Linux: The Complete Reference*, McGraw Hill, 6th Edition, 2008.

e-Resources:

https://www.classcentral.com/course/youtube-electronics-linux-programming- scripting-47539

Course Outcomes:

- Gain fluency in programming with scripting languages (PERL, TCL, PYTHON).
- Create and execute scripts in PERL/TCL/PYTHON for CAD tool automation and data handling.
- Demonstrate scripting in PERL/TCL/PYTHON for system-level and web applications.
- Analyze security issues, advanced data structures, and tool interfacing using scripting languages.

	L	T	P	C
M. Tech I-Year II- Semester	3	1	0	4

Network Security and Cryptography

(Professional Elective-IV)

Course Objectives:

- To understand the fundamental concepts of cryptography and network security mechanisms.
- To explore classical and modern encryption algorithms and their security properties.
- To learn public key cryptographic systems, key exchange protocols, and associated number theory.
- To understand message authentication, digital signatures, and secure communication protocols.
- To study real-world network security applications such as IP security, web security, email security, and threat mitigation.

UNIT- I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques. Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

UNIT-II:

Encryption Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers. Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation. 12 3 Public Key Cryptography: Principles, RSA Algorithm, Key Management.

UNIT-III:

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography. Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT-IV:

Message Authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. Hash and Mac

Algorithms. MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-V:

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms Intruders, Viruses and Related threats. Fire Walls: Fire wall Design Principles, Trusted systems.

Textbooks:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

Reference Books:

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.
4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

e-Resources:

https://nptel.ac.in/courses/106105031

Course Outcomes:

- Explain the fundamental principles of cryptography and classical encryption techniques.
- Apply symmetric and asymmetric encryption algorithms in securing data communication.
- Analyze and evaluate cryptographic techniques such as RSA, Diffie-Hellman, and digital signatures for secure systems.
- Design and implement secure communication mechanisms using protocols like SSL, IPsec, and authentication systems.

	L	T	P	C
M. Tech I-Year II- Semester	0	1	2	2

Embedded Systems Design Lab

Course Objectives:

- To acquire working knowledge of various embedded development tools.
- To develop and implement sample programs on ARM-based processors or equivalent.
- To create applications using the ARM processor in an IDE environment with RAM tool chain and libraries.
- To design and implement embedded applications with peripheral interfacing.
- To develop advanced embedded system applications using ARM processors.

Note:

- The following programs are to be implemented on ARM based Processors/Equivalent.
- Minimum of 10 programs are to be conducted.

The following Programs are to be implemented on ARM Processor:

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches.
2. Write an Assembly programs to configure and control General Purpose Input/ Output (GPIO) port pins
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file.
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment.
6. Program to demonstrate a simple interrupt handler and setting up a timer.
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface.
9. Program to implement Buzzer Interface on IDE environment.
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment.
12. Program to demonstrate I2C Interface – Serial EEPROM.
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal.
15. Program to demonstrate SD-MMC Card Interface.

Course Outcomes:

- To gain the working knowledge of various embedded tools.
- To develop sample programs to be implemented on ARM based Processors or equivalent.
- Create applications for using the ARM Processor on IDE Environment using RAM Tool chain & Library.
- Develop applications using the concept of Interfacing.
- Design advanced embedded applications using ARM Processor.

M. Tech I-Year II- Semester	L	T	P	C
	0	1	2	2

VLSI Design Lab

Course Objectives:

- Gain practical experience in designing and simulating CMOS digital and analog circuits using EDA tools.
- Implement combinational and sequential logic circuits at the transistor level through schematic and layout design.
- Understand the full-custom VLSI design flow, including DRC, LVS, and post-layout simulation.
- Analyze and optimize CMOS circuit performance in terms of power, delay, and area.

List of Experiments

1. Design and Simulation of Basic Logic Gates using CMOS Logic (AND, OR, NOT, NAND, NOR, XOR, XNOR)
2. Design and Implementation of Half Adder and Full Adder using CMOS
3. Design and Implementation of Half Subtractor and Full Subtractor using CMOS
4. Low-Power Design of 4:1 Multiplexer and 1:4 De-Multiplexer Using 6T Logic
5. Design of 4:2 Encoder using CMOS Logic
6. Design of 2:4 Decoder using CMOS Logic
7. Design of a 2-Bit Comparator using CMOS Logic
8. Implementation of Boolean Expressions Using CMOS Logic circuit
9. Design and Simulation of Flip-Flops using CMOS Logic (SR, JK, D, and T Flip-Flops)
10. Design and Analysis of SRAM Using CMOS Technology
11. Design and Analysis of DRAM Using CMOS Technology
12. Design of a CMOS Ring Oscillator for On-Chip Frequency and Delay Characterization

Course Outcomes:

- Design and implement basic logic gates using CMOS technology.
- Develop and simulate combinational and sequential digital circuits at the transistor level.
- Design and analyze sequential circuits such as latches and flip-flops using CMOS logic.
- Create transistor-level schematics and basic layouts for CMOS circuits using EDA tools like Cadence Virtuoso.
- Understand the fundamentals of layout design and gain introductory experience in drawing layouts of MOS transistors and basic CMOS circuits.

M. Tech II Year I- Semester	L	T	P	C
	2	0	0	2

Research Methodology and IPR
(Open Elective)

Course Objectives:

- Understand the basics of research and its types.
- Learn how to define research problems and hypotheses.
- Study data collection, analysis, and interpretation methods.
- Gain knowledge of intellectual property rights and types.
- Understand the process of patent filing and copyright protection.

Unit I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit II:

Effective literature studies approach, analysis Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit III:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit IV:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit V:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'""
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step-by-Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

Course Outcomes:

- Identify research problems and formulate research questions.
- Apply suitable methods for data collection and analysis.
- Write and present effective research reports.
- Explain various forms of IPR and their importance.
- Describe procedures for patent and copyright applications.