JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURAJADA VIZIANAGARAM

JNTU-GV COLLEGE OF ENGINEERING, VIZIANAGARAM
DWARAPUDI, VIZIANAGARAM, ANDHRA PRADESH, INDIA
www. jntugvcev.edu.in

A Three-Day National Level Workshop On

Analog and Digital CMOS VLSI Design Using Microwind EDA Tool

(02nd to 04th November 2023)

Organized by
Department of Electronics and Communication Engineering
In association with

and

Faculty Development Cell –JNTUGV-Vizianagaram

About the Institution:

Jawaharlal Nehru Technological University Gurajada Vizianagaram (JNTUGV) is established in the year 2022 under Act No. 22 of 2021 Govt. of AP. JNTUGV College of Engineering Vizianagaram, is one of the constituent engineering colleges of this University (JNTUGV) playing a significant role in imparting technological education in the state of Andhra Pradesh. The institute offers seven (07) UG (B. Tech) programmes Viz., CE, EEE, ECE, CSE, IT, ME and Metallurgical engineering and five (05) PG (M. Tech) programmes Viz., EEE, ME, ECE, CSE, IT, apart from MCA.

About the Department:

The department of ECE offers U.G & P.G courses with an intake of 60 and 18 students respectively. It has excellent infrastructural facilities and well equipped with full-fledged Laboratories, audio visual and software tools such as MULTISIM, Active HDL, MATLAB, IAR embedded workbench, image processing software's and 10 Mbps internet facility. Right from the inception the department works with an objective provide the best quality technical education at graduate and post graduate levels. In addition to this the department also encourages research and development, Consultancy and interaction with industry to achieve academic excellence.

Chief Patron:

Prof. Dr. K. Venkatasubbaiah
Hon'ble Vice Chancellor, JNTUGV Vizianagaram.

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Prof. K. Sri Kumar
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Convenor:

Dr. B. Nalini,
Head of ECE Department, JNTUGV CEV, VIZIANAGARAM

Workshop Coordinators:

1. **Dr. G. Appalanaidu**
   Assistant Professor, ECE Department
2. **Sri. China Raju Manda**
   Assistant Professor (C), ECE Department

Organizing Committee:

1. **Dr. K. Babulu, Professor**
2. **Dr. K. Chandrabhushana Rao, Professor**
3. **Sri. R. Gurunadha , Associate Professor**
4. **Dr. T. S. N. Murty, Assistant Professor**
5. **Dr. M. Hema, Assistant Professor**
6. **Sri. K. V. Raju, Assistant Professor (C)**
7. **Sri. J. Sateesh, Assistant Professor (C)**
8. **Sri. K. V. Satyanarayana, Assistant Professor (C)**
9. **Smt. V. Vijaya Santhi, Assistant Professor (C)**
10. **Smt.M. Krishna Priya, Assistant Professor (C)**
11. **Smt. K. Anusha Yadav , Assistant Professor (C)**

About the Workshop:

The increasing trend towards enhanced integration at all levels of Electronics Design has resulted in the development of larger integrated circuits, accompanied by a continuous reduction in feature size. The exponential increase in feature sizes within semiconductor technologies has many implications for layout optimization. These implications are associated with noise, interconnect delay and crosstalk, parasitic effects, and power dissipation. These impacts challenge the reliability of certain assumptions.

Therefore, the reduction in size and the growing complexity of Microelectronics Applications necessitate innovative integration methods and a more thorough understanding of the physical components of VLSI design. The field of Electronic Design Automation (EDA) has experienced significant growth in parallel with the continuous downsizing of semiconductor technology.

Using EDA tools has become essential in the design process of very large-scale integration (VLSI) circuits. This workshop aims to provide participants with a comprehensive understanding of VLSI design and practical exposure to µWIND, a layout and simulation tool utilised in deep submicron CMOS design. The attendees will be equipped with an opportunity to gain knowledge and understanding in CMOS Design and Technology, Circuit Design, Simulation, and Layout Design through lectures offered by esteemed experts in VLSI design.

Objectives:

- Introduction to CMOS VLSI design issues
- Problem-based learning on MoS devices, introducing width/length effect, Ion/Ioff and Vt illustration, for both N and P devices.
- To design of inverters and oscillators and
- To design interconnects, introducing design strategies, and impact on switching speed and power consumption.
- To design of analog blocks introducing amplification, voltage reference, addition of analog signals, and mixed-signal blocks Demonstration of µWIND CMOS layout tool
- Hands-on experience on µWIND tool

Topics to be Covered:

Day 1:

- Introduction to ASIC and FPGA Design Flows Difference between ASIC & FPGA.
- Design Trends in Deep-Submicron technologies
- Introduction of Backend Tool, CMOS design concepts, basic circuit building
- Hands on Session Analysis of CMOS Inverter

Day 2:

- Introduction to SPICE Coding (Win SPICE)
- Introduction to Microwind Layout tool
- Conversion of Schematic to Layout
- Analysis of Layout design through simulation
- Physical Verification
- Parametric Analysis
- Delay, Crosstalk, DRC and ERC Analysis
- Hands on Session on SPICE and Microwind tool

Day 3:

- Technology scale down and its impacts on device integration, performance and design challenges
- Introduction to FinFET technology
- Current trends in 7 - 5 nm FinFET cell design
- Current trends in 3 nm NSFET cell design
- Hands on Session Schematic and Layout design

Targeted Participates :

Interested Faculty, PG and Ph.D scholars of ECE, CSE, EEE and related departments are eligible, can register by completing the online Google form:

Resource Persons :

- **Vinay Sharma, Head – Microwind,India**
- **Dr. N. BalaDastagiri, TM, TechFLUENT sol. Pvt. Ltd**
- **Srikanth A, TM, Microwind, India**

Important Information:

- ✓ Total numbers of seats are limited to 60.
- ✓ There is a registration fee of **Faculty: Rs.300/-. PG Students :Rs.200/-**
- ✓ The shortlisted candidates will get a selection notice by E-mail and are expected to attend the workshop offline at JNTUGV CEV VIZIANAGARAM.
- ✓ Regarding payment of fee, scan the QR code and upload the receipt in the Google form. *https://docs.google.com/forms/d/e/1FAIpQLScfvdL1WpZ99O9ztr-b46Nktj_qWI2YwjLmhV5_oPsX2I-gDA/viewform?usp=sf_link*

Important Dates:

Last date for Registration: 28-10-2023
Notification of Selection: 31-10-2023
Workshop Period : 02nd to 04th -November -2023

Venue:

Academic Block-II, ECE Department , JNTUGV CEV VIZIANAGARAM

For any query, please contact:

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